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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,776	03/10/2004	Brad Underwood	200313420-1	4159

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,776	UNDERWOOD ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Amendment filed on 9-6-05 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained as indicated below.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "signals", lines 10 and 11 of claim 1, lacks antecedent basis. It appears that each signal source provides a single signal as. Claim 20 has the same issue as that of claim 1.

As to claim 3, the limitation "said controlling signals", line 2-3, lacks antecedent basis.

As to claims 2 and 4-11, they are rejected for being dependent on the rejected claims as noted above.

As to claim 21, it is unclear if the limitation "a control signal", line 15, is related to that of lines 4-5 and lines 7-8.

As to claims 22-23, they are rejected for being dependent on the rejected claims as noted above.

As to claims 24-26, each of the limitation "a control signal", four places, recited in these claims has the same issue as noted in claim 21. Further, the limitation "a fourth system node" of claim 26, lacks antecedent basis since there is no "a third system node" recited earlier.

As to claim 27, the limitation "multiple signals" is not understood since it is inherent that a MUX receives multiple input signals. Further, the limitation "the signals", line 3, lack antecedent basis.

As to claim 28, it is rejected for being dependent on the rejected claim as noted above.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-8, 12-18, 20-22 and 27-28, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by the Doblar reference (U.S. Patent 6,194,969).

Doblar discloses in figures 1 and 2 a distributed redundant control signal distribution system comprising a first control signal source 220A co-located with a first set of control signal (i.e., inputs of MUX on clock board 105A) controlled circuit elements (i.e., components on system board 120, fig.1), at least one second control signal source 220B co-located with a second set of control signal (i.e., inputs of MUX on clock board 105B) controlled circuit elements (i.e., components on system board 120, fig.1); a first controller (i.e., portion of system controller 110 in fig. 1 receiving signal from 105B) and at least one second controller (i.e., portion of system controller 110 in fig. 1 receiving signal from 105A); said controller operable for substituting signal from said second control signal source for signals from said first control signal source if

said signal from said first control signal source become unavailable to either said first or second circuit elements (See col. 3, lines 12-26) as required by claim 1.

As to claim 2, the control signal sources 220A-B are seen as system clock as disclosed in ABSTRACT of the Patent.

As to claim 3, fig.2 shows the first and second sets of circuit elements are interconnected by at least two transmission paths (106A; 106B) and wherein said controlling signals travel over both of said transmission paths by means of FANOUT BUFFER.

As to claim 4, fig. 1 and col. 3, lines 27-35 disclose the one controller enables said controlling signals to control both sets of controlled circuit elements even when one of said transmission paths is inoperative.

As to claim 5, it is understood that a MUX is for switching between its inputs. Therefore, it is inherent that the system controller 110 of Doblar comprising a multiplexer for accepting signals on its input from said first and second control signal sources, said multiplexer operable for selecting which one of said control signals controls said controlled circuit elements since col. 3, lines 20-22 disclose the system controller 110 switches between control signal 106A and 106B.

As to claim 7, col. 3, lines 27-35 disclose the MUX (i.e., controller) co-located with the first set of controlled circuit elements.

As to claim 8, the scope of claim is similar to claim 7. Therefore, it is rejected for the same reasons set forth above. It is noted that col. 3, lines 27-35, indicates that there exists a controller on each board.

As to claims 12-15, they are rejected for reciting method/step derived from the apparatus of claims 1-5 and 7 which are rejected as noted above.

As to claim 16, Doblar discloses in figure 2 a system for controlling clock signals for a plurality of electronic boards comprising a clock source (220A or 220B) on at least two of said electronic boards (105A and 105B); at least one signal (106A or 106B) connection between all of said electronic boards, each said signal connection allowing clock signals to pass between said plurality of boards; a controller on each of said boards (col. 3, lines 27-35), said controller operable for hierarchically selecting clock signals from at least one of said signal connections (i.e., selecting either master or slave clocks); and wherein said signal controllers on said first and second electronic boards are further operable for hierarchically selecting one or the other of said clock sources (i.e., output of VCXO or OTHER SOURCE CLOCK).

As to claim 17, fig. 1 and col. 3, lines 27-35 disclose the hierarchy is such that said controllers only select the clock source from said second one of said boards when the clock source from said first one of said boards is not available.

As to claim 18, the argument for rejecting claim 5 noted above is also applicable herein.

As to claim 20, it is rejected for reciting method/step derived from the apparatus of claim 21 which is rejected as noted above.

As to claim 21, figure 1 and 2 disclose a first system node (CLOCK BOARD 0), comprising a control signal source 220A, a controller (i.e., portion of system controller 110 in fig. 1 receiving signal from 105A), an input (i.e., output 106B from CLOCK BOARD 1), an output (i.e., signal 106A provided to input of CLOCK BOARD 1) and a first set of circuit elements (i.e., components on system board 120, fig.1) requiring a control signal (106A supplied

to 120); and a second system node (CLOCK BOARD 1), comprising a control signal source 220B, a controller (i.e., portion of system controller 110 in fig. 1 receiving signal from 105B), an input (i.e., output 106A from CLOCK BOARD 0), an output (i.e., signal 106B provided to input of CLOCK BOARD))and a second set of circuit elements (i.e., components on system board 120, fig.1) requiring a control signal (106B supplied to 120); wherein the output of the first node is coupled to the input of the second node (as shown and explained above); wherein the output of the second node is coupled to the input of the first node (as shown and explained above); and wherein the controller of the first node operates in tandem with the controller of the second node to alternatively select between the control signal sources of the first and second node to supply a control signal to the first set and second set of circuit elements (See Abstract).

As to claim 22, the control signal sources 220A-B are seen as system clock as disclosed in ABSTRACT of the Patent.

As to claim 27, it is understood that a MUX is for switching between its inputs. Therefore, it is inherent that the system controller 110 of Doblar comprising a multiplexer for accepting signals on its input from said first and second control signal sources, said multiplexer operable for selecting which one of said control signals controls said controlled circuit elements since col. 3, lines 20-22 disclose the system controller 110 switches between control signal 106A and 106B.

As to claim 28, it is rejected for reciting a basic operation of a MUX since the output of a MUX is predetermined by its control signal to select a particular input terminal to be coupled to the output of a MUX.

Response to Arguments

5. Applicant's arguments filed 9-6-05 have been fully considered but they are not persuasive.

Regarding the rejection of claim 1, Applicant has argued that Doblar does not disclose the following limitations:

- a single controller with portions comprised on separate boards is not two controllers; and
- a first control signal source co-located with a first set of control signal controlled circuit elements; at least one second control signal source co-located with a second set of control signal controlled circuit elements.

Examiner respectfully disagrees with the above assertions since system controller 110 of Doblar is seen as comprised two controllers wherein each receives separate signal from separate clock source. Further, column 3, lines 31-32, discloses "*a portion of the system controller 110 may be comprised on each board, even when not expressly illustrated*". Therefore, Doblar clear teaches a first controller and second controller.

The recitation of claim merely calls for various components being co-located with respect to each other. There is no recitation of distinct locality of the first and the second control signal sources. In fact, the location of a certain component within a circuit is not given patentable weight since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japiske, 86 USPQ 70.*

Regarding the rejection of claim 12, Applicant has argued that Doblar does not disclose the control signal sources located on the same board. Examiner respectfully disagrees since

element 120 of Doblar is disclosed as a generalized computer system board which may have more than one boards (col. 3, lines 6 and 58-60). Again, the location of a certain component within a circuit is not given patentable weight since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japiske, 86 USPQ 70.*

Regarding the rejection of claim 16, Applicant has argued that "a single controller with portions comprises on separate board is not two controllers". Examiner respectfully disagrees since Doblar discloses a system controller 110 having more than one portion controller. Therefore, each portion controller can be called or labeled controller.

Regarding the rejection of claim 20, Applicant has argued that "*components on system board 120 are on a different board than the clock sources which are located on the clock boards 105A and 105B*". Examiner respectfully disagrees since Applicant's argument is irrelevant with respect to the recitation on claim. It is noted that each and every component of Doblar's circuit is seen as "local", "next to", "adjacent" or "nearby" with each other. Again, the location of a certain component within a circuit is not given patentable weight since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japiske, 86 USPQ 7.*

Allowable Subject Matter

6. Claims 6, 9-11, 19 and 23-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus and method thereof comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the following limitations:

- The multiplexer has a preset hierarchically control among its respective inputs as required by claim 6.
- At least a third set of control signal controlled circuit elements wherein signals from said first control signal source control said third set of controlled circuit elements, said third set of controlled circuit having co-located therewith a controller for substituting signals from said second control signal source for said signals from said first signal control source if said signals from said first signal control source become unavailable as required by claims 9, 23 and 26. And
- The at least one signal connector is a plurality of independent transmission paths; and wherein said controllers accept signals from each of said transmission paths for said hierarchical selection as required by claim 19.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
10-18-05

Kenneth B. Wells
Primary Examiner